What is claimed is:

1. An apparatus comprising:

an execution unit to execute an instruction;

a replay system to replay an altered instruction if the execution unit executes the instruction erroneously.

2. The apparatus of claim 1 wherein the replay system comprises:

a replay loop to replay the instruction under a first condition; and

an instruction morphing circuit to replay the altered instruction under a second condition.

3. The apparatus of claim 1 wherein the replay system comprises:

a replay loop to replay the instruction if the instruction is a first instruction; and

an instruction morphing circuit to replay the altered instruction if the instruction is a second instruction.

4. The apparatus of claim 3 wherein the first instruction is one of a plurality of non-modifiable instructions and the second instruction is one of a plurality of modifiable instructions.

5. The apparatus of claim 4 wherein the plurality of modifiable instructions are morphed only if a failure in their initial execution occurs.

6. The apparatus of claim 1 wherein said replay system tracks at least one extra bit to allow alterations of instructions.

7. The apparatus of claim 1 wherein said apparatus comprises a low level cache and a higher level cache, wherein the replay system is to alter a load instruction that has already missed in the higher level cache to thereafter only access the low level cache.

8. The apparatus of claim 1 wherein said apparatus comprises a page miss handler to handle instructions that cause page faults, wherein the instruction is a memory access that causes a page fault, and wherein the replay system is to change the memory access to one or more memory accesses to handle the page fault.

9. The apparatus of claim 8 wherein the replay system is to replace the memory access with a page descriptor read, then to replace said page descriptor read with a page table entry read, then to reinstate the memory access.

10. The apparatus of claim 1 wherein said instruction is a dependent instruction that is dependent on a result from a previous instruction, and wherein the replay system is to alter the dependent instruction to avoid execution in further iterations through the replay system until the previous instruction has successfully executed.

11. The apparatus of claim 10 wherein the replay system is to alter the dependent instruction by setting a valid bit for the dependent instruction to indicate that the

instruction is invalid.

12. The apparatus of claim 10 wherein the replay system is to alter the dependent instruction back into an executable form when said previous instruction retires.

13. The apparatus of claim 11 wherein the replay system is to reset the valid bit when any instruction retires.

14. The apparatus of claim 10 wherein the replay system is to track a sequence number for the previous instruction and wherein the replay system is to return the dependent instruction to an executable form when said previous instruction completes.

15. The apparatus of claim 10 wherein the apparatus further includes a cache, and wherein the replay system is to return the dependent instruction to an executable form when a write to the cache occurs.

16. The apparatus of claim 1 wherein said instruction is a high precision instruction and said replay system is to generate a first result and then the altered instruction is to be executed to generate a final result from the first result.

17. The apparatus of claim 1 wherein said execution unit is a numeric execution unit and wherein said replay system is to a detect data dependent condition for the instruction and to provide the altered instruction to achieve an identical result.

18. The apparatus of claim 17 wherein the instruction is a rounding instruction and the altered instruction is an add instruction.

19. The apparatus of claim 17 wherein the numeric execution unit lacks hardware to compute one or more relatively rare numeric cases and wherein such relatively rare numeric cases are instead implemented by injecting, via the replay system, the altered instruction to achieve an effectively identical result.

20. A processor comprising:

a scheduler to dispatch an original instruction;

an execution unit to attempt execution of the original instruction;

a checker to determine whether the original instruction executed properly;

a replay system comprising:

a replay loop to replay the original instruction;

a morphing circuit to change the original instruction into an altered instruction and to replay the altered instruction.

21. The processor of claim 20 wherein said replay system is coupled to replay the original instruction when a first condition occurs and to replay the altered instruction when a second condition occurs.

22. The processor of claim 20 wherein said replay system is coupled to replay the original instruction when the original instruction is a first instruction and to replay the altered

instruction when the original instruction is a second instruction.

23. The processor of claim 22 wherein said first instruction is one of a plurality of non-alterable instructions and wherein said second instruction is one of a plurality of alterable instructions.

24. A method comprising:

executing an original instruction;

determining if a first condition occurs;

if said first condition occurs, then

morphing said original instruction to form a morphed instruction; and

executing said morphed instruction.

25. The method of claim 24 wherein determining if the first condition occurs further comprises:

determining whether the original instruction executed improperly.

26. The method of claim 24 further comprising:

determining whether a second condition occurs;

if said second condition occurs, then

replaying said original instruction for execution.

27. The method of claim 24 wherein morphing comprises:

altering a load instruction that has already missed in a higher level cache to thereafter only access a lower level cache.

28. The method of claim 24 wherein morphing comprises:

altering a page-fault-causing instruction to perform one or more other instructions to handle a page fault.

29. An article comprising a machine readable medium that stores data representing an integrated circuit comprising:

an execution unit to execute an instruction;

a replay system to replay an altered instruction if the execution unit executes the instruction erroneously.

30. The article of claim 29 storing further data representing the integrated circuit, which further comprises:

a replay loop to replay the instruction under a first condition; and

an instruction morphing circuit to replay the altered instruction under a second condition.

31. The article of claim 29 wherein the data representing the integrated circuit comprises a functional description of the integrated circuit.

32. The article of claim 29 wherein the data representing the integrated circuit comprises

a hardware description language code.

33. The article of claim 29 wherein the data representing the integrated circuit comprises data representing a plurality of mask layers string physical data representing the presence or absence of material at various locations of each of said plurality of mask layers.

34. An article comprising a machine readable carrier medium having stored thereon data which, when loaded into a computer system memory in conjunction with simulation routines, provides functionality of a model comprising:

an execution unit to execute an instruction;

a replay system to replay an altered instruction if the execution unit executes the instruction erroneously.

35. The article of claim 34 wherein the model further comprises:

a replay loop to replay the instruction under a first condition; and

an instruction morphing circuit to replay the altered instruction under a second condition.